REVOX C-270
C-270 TC - C-274 - C-278
TLS-4000

INTERFACE DOCUMENTATION

Interface number : 1.812.404.21
IF - Doc number : 10.27.1621

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TECHNICAL DOCUMENTATION
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printed in Switzerland
Order No.: 10.27.1621 (Ed. 0292)

Summary

1 General Information

1.1 Ordering Information

	Order number
■ Interface Set (including Interface, Cable and Documentation)	21.812.404.21
■ Interface Board (Hardware/Software)	1.812.404.21
■ Hardware: TLS Parallel Interface	1.812.491.20
■ Software Set	1.812.915.21
■ IF-Cable 5m	1.023.768.00
■ Interface Docu-number	10.27.1621
■ Hardware (parallel IF) Docu-number	10.27.3040

1.2 Slave Model

- REVOX C270 TC, C274, C278
- Device with compatible connection: -

1.3 Software

■ First release (index 20)	1.812.951.20 (26/90)
■ Structure update	1.812.951.21 (21/91)

2 Installing Procedures

2.1 TLS 4000 Requirements

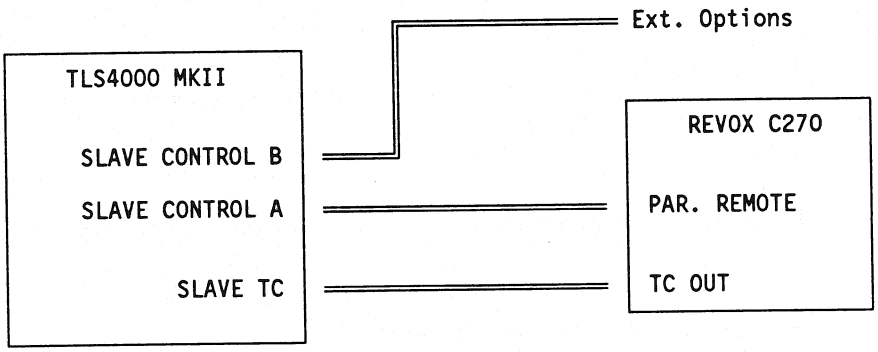
Order number

- Synchronizer Board — 1.812.320.24 or later
- Interface: — right set up of the DIL-SWITCHES (see section 3.3)

2.2 Slave Requirements

- The jumpers on the input board of the C270 have to be switched to SYNC.
- Position of the slave DIL-SWITCH: (see slave manual)
  Nr.1 OFF \ Nr.8 ON (external varispeed on)

2.3 Connection Slave-Synchronizer



2.4 Quick Test, Adjustments

Put the TLS 4000 MKII to power off. Take the interface and put it to the right place in the synchronizer. Make shure that the connection between the synchronizer and the slave is correct and switch power on.
During the first 5 seconds the interface will make a selftest. This phase will be commented by some LED messages. After this 5 seconds the LED display will be free for all the other messages. (see section 3.5)

After disconnecting the time code line and with the slave in play mode you can easily check that the move information is available at the input of the synchronizer. Just have a look at the time code display of the LCU or the controller. It must be counting in the right direction with the right speed.

Test if a proper SMPTE time code is avaiable on slave and on master tape.

No adjustments are necessary.

3 Operating Instructions

3.1 Technical Specifications

- Slave type:
  - SMPTE/EBU - TC machine with move pulse information
  - No code during wind modes
  - GOTO function with PLAY - STOP sequenze
  - Parking in LOCK in advance.
  - CHASE-PLAY with preparking.
- Link type: parallel (PLAY, STOP, FWD, RWD,REC)
- Capstan control: frequency control (9600 Hz nominal)
- Movepulse information: Clock and direction

Direction : LOW = forward
Clock : The frequency depends on the nominal speed

3.75	ips	:	8 Hz
7.5	ips	:	16 Hz
15	ips	:	32 Hz

- Lock time (typ): (in CUED status, Master Start - SYNC): 2 sec
  (in CHASE 10*vnom, Master Start-SYNC): 10 sec
- Drop-In Delay: compensated
  Drop-Out Delay: compensated
- TC Compensation: C270TC with slave internal compensation
  C274/C278 not necessary
- Wow & Flutter: less then 20% higher than the values of the slave (typically within the slave rates)

Park accuracy: typ. 40 ms
Sync accuracy: typ. 40 us

3.2 Summary of Supported Functions

Operating conditions:

- STOP
- PLAY — nominal (internal reference) or ext. varispeed
- REC — (TLS reference ± 50 %)

- EDIT — same as STOP
- FORW, REW — Variwind continuously from 0 to .. vmax
- SHTLF, SHTLR — same as FORW,REW

- LOC, LOCREL — made by interface

- MUTE: — not implemented

- REHEARSE: — available with PLAY instead of REC (see DIL-SWITCH 2, section 3.3)

- EVENT Relay: — There is a relay available for the user. The relay can be switched on by the EVON synchronizer command and off by the EVOFF command. (see 3.4)

- CONDITIONAL COMMANDS: — are available for STOP..REW, DROPIN, DROPOUT, EVON, EVOFF

- STATUS Request: — The status information is requested and updated through the parallel communication link by the interface software. Additional information about nominal speed is available for the synchronizer via the move pulse connection. The C270-TC does not have a "tapeout" status. Instead of this the C270-TC answers with a "stop" status.

- Audio-TC-channel setup — not implemented.

- TRANSPARENT Commands — not implemented.

- KEYBOARD DISABLE — Not implemented.

3.3 DIL-SWITCH Functions

The following functions are controlled by the DIL SWITCH SZ81:

- Switch 1: Active polarity of the RECEN signal.
  OFF : recording mode enabled with RECEN LOW
  ON : recording enabled with RECEN HIGH or open

- Switch 2: Rehearsal mode
  If the rehearsal mode is active, RECORD commands will be
  OFF : replaced by PLAY commands
  ON : directly passed to the slave

  This switch will be off when there is no external REHEARSAL circuit (controled by the signal B-REHR at SLAVE CONTROL B). So you can be shure, than no RECORD command will be given to the slave during the rehearsal mode.
  The position of the DIL-SWITCH will only be checked just after switching on the rehearsal mode. If you change the position of this switch, it is necessary to switch on the rehearsal mode one more time.

- All other switches are not used, but they should be in "off" position to guarantee compatibilily with later software versions.

- Default Settings: all switches in OFF position

3.4 Additional Features at Slave Control B Connector

RECEN (PIN 2):
Hardware record enable. The function of this input is defined by DIL-SWITCH 1 (refer to section 3.3).

REL1 (PIN6), REL2 (PIN7):
This relay contact can be used for any general purpose.
It has to be turned ON and OFF by the EVON and EVOFF synchronizer commands.

B-REHR (PIN8):
Output of the rehearse status (open collector, active low).
It is switched active by the RHRSON synchronizer command.

SREHSL (PIN 12):
TTL compatible input for switching on the rehearsal mode.

HIGH (OR OPEN):	REHEARSAL OFF
LOW:	REHEARSAL ON

MVCL (PIN21), MVDR (PIN24):
This output (open collector) provides slave movepulse information for external use.
MVCL: The frequency depends on the nominal speed
MVDR: LOW = forward

3.75 ips : 8 Hz
7.5 ips : 16 Hz
15 ips : 32 Hz

XVSENB/XVSREF (PIN 5, PIN 3):
An external varispeed circuit can be connected to the Slave Control B connector. The two signals are switched to the slave during the OFF-mode of the synchronizer.

PAIN 9	LOW = varispeed enable
PAIN 10	reference frequency (nominal 9600 Hz)

3.5 LED Diagnostic Display

Three LEDs are situated at the front of the interface board. They provide information about the result of the initial selftest and the online status.

DL 1 2 3 **(Front view)**
(# = LED blinking, - = LED off, * = LED on)

- An initialization procedure is executed after reset and the main hardware devices are tested. Any resulting error is signalled with a blinking left LED (DL1, about 1 Hz).

- If all LEDs are blinking, the internal EEPROM of the processor has to be reconfigured. This should only happen if the processor war replaced and the interface switched on for the first time. If this happend, you have to switch JS 1 to position AB and reset the interface (power off - power on). After the initialisation the three LEDs should blink again. Put JS 1 back to position BC and reset the interface again.
  Now the 68HC11 should be reconfigured and the LED message should not be the same.

DL1	DL2	DL3	
#	-	-	CPU RAM test failed.
#	-	*	RAM test failed.
#	*	-	SSDA test failed.
#	#	#	Microprocessor 68HC11 has to be reconfigured

- If no error was found, DL1 stays dark and the other two LEDs light, if communication with the slave or the synchronizer fails.

DL1	DL2	DL3	
-	*	*	no connection with the synchronizer board
-	#	-	no connection with the SLAVE

- If the left LED is on, a fatal processor error has occurred. A reset is necessary to return to operation mode. The interface board should be checked whenever such an error was encountered.
  In this case the interface should be resetted and this error message should not occur anymore.

DL1	DL2	DL3	
*	-	-	Fatal soft- or hardware error (eg ROM defect)
*	-	*	Watch dog error
*	*	-	Clock error
*	*	*	Illegal opcode

3.6 Applications Hints

- Move pulse information may be wired to "master tallies" inputs of further synchronizer, if the C270 is master (section 3.4).)

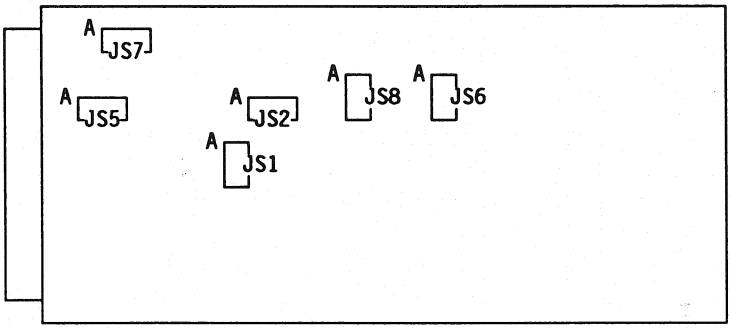
- With a C270TC it is recommended to run with 7.5 or 15 ips, because of the poor time code quality provided by the internal time code processor.
  There are no restrictions with the C274 or C278, because time code is recorded on any of the audio tracks.

- Since the C270 TC doesn't provide a 'Tapeout' status, the interface can not recognize it ande reads a 'STOP'. If a 'Tapeout' occurs during locating or chasing, it is recommended to switch the synchronizer to OFF before loading the tape again. After the new loading put the slave to 'PLAY', so that the synchronizer can read timecode.

- The interface can support an external rehearse circuit.
  (see 3.4)

4 Service Instructions

4.1 Jumper Settings



Functions of jumpers:

	Position AB	Position BC
JS1	Processor in special test mode	Processor in normal expanded mode *
JS2	PE6 input of the processor is LOW	PE6 input of the processor is HIGH *
JS5	IF ground is connected to the slave ground *	No connection between IF ground and slave ground
JS6	Capstan reference output has no pullup resistor	Capstan reference output has a pullup resistor *
JS7	Opto isolated inputs are supplied from the IF	Opto isolated inputs are supplied from the slave *
JS8	Capstan pullup resistor is supplied with 5V (or MVCC if JS7 'AB')*	Capstan pullup resistor is supplied with 15V

* Default settings for REVOX C270

4.2 Signal Description, Slave Connectors

SLAVE CONTROL A:

Pin	Signal	Type	Slave Sig.	Description
1	MGND		0.0 V	ground of C270
2	PAIN1	I in	BR-REW	Rewind status
3	PAIN2	I in	BR-FORW	Forward wind status
4	PAIN6	I in	-	(not used)
5	CAPEN	I out	SR VRSPD	capstan varispeed enable (LOW = enb)
6	-		-	
7	MOVCL	I in	OR-MVCLK	move signal clock from C270
8	-		-	
9	PAIN5	I in	BR-REC	Record status
10	MOVDIR	I in	OR-MVDIR	move signal direction from C270
11	+5V		-	IF power supply
12	0.0V		-	screen
13	CAPCL	I out	IR-FEFEX	capstan clock (9600Hz nominal)
14	-		-	
15	PAIN3	I in	BR-PLAY	PLAY status
16	PAIN4	I in	BR-STOP	STOP status
17	PAOUT7	I out	-	(not used)
18	PAOUT8	I out	-	(not used)
19	PAOUT5	I out	SR-REC	Record command
20	PAOUT1	I out	SR-REW	Rewind command
21	PAOUT2	I out	SR-FORW	Forward wind command
22	PAOUT3	I out	SR-PLAY	PLAY command
23	PAOUT4	I out	SR-STOP	STOP command
24	-		-	
25	MVCC	+ 24 V	+ 24.0	supply voltage of C270

I out logic output, active low
(open collector, max 30V/0.3A)

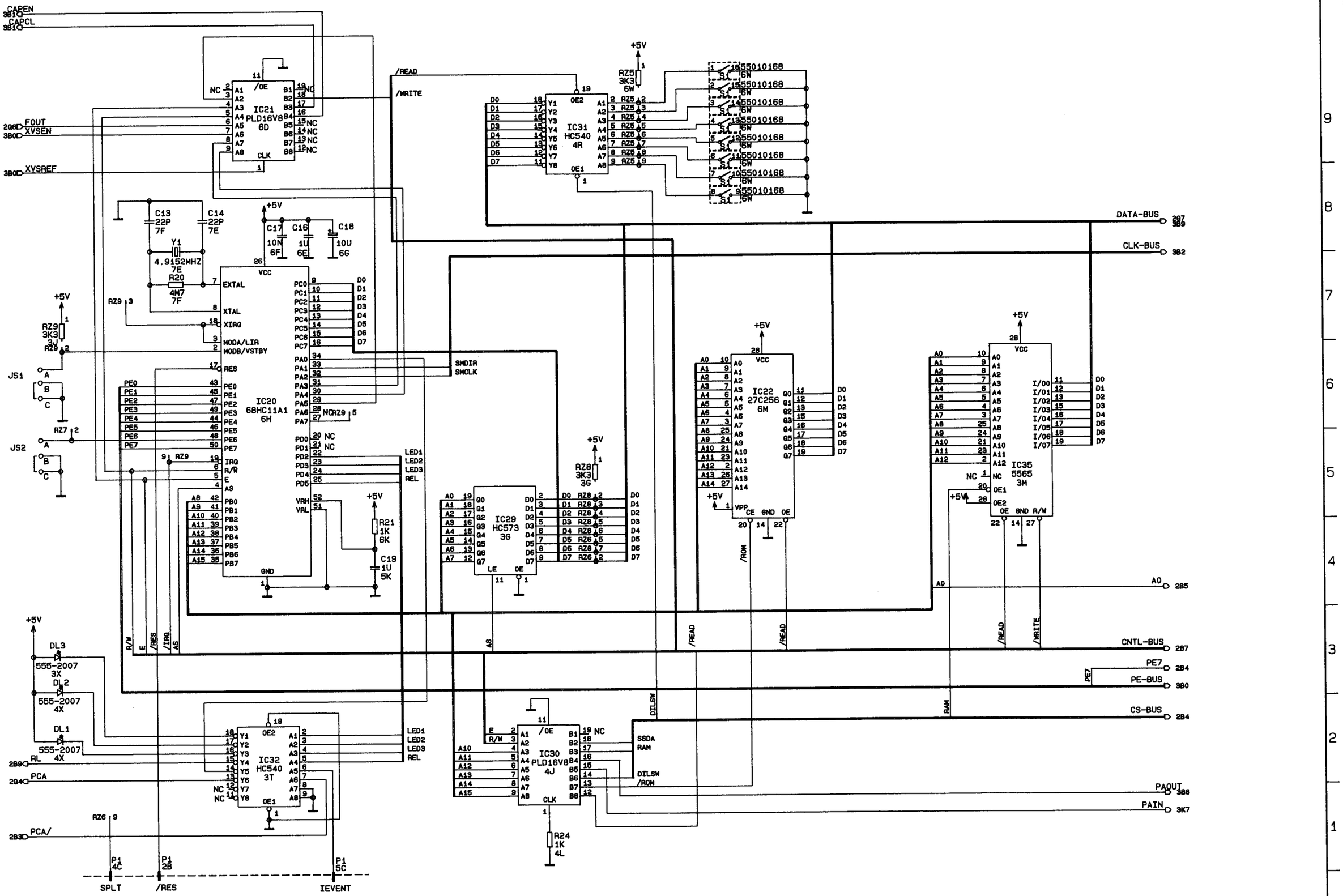
I in logic input, active low, optoisolated
(I-low > 10 mA)

SLAVE CONTROL B:

Pin	Signal	Type	Slave Sig.	Description
1	0.0 V			signal ground
2	RECEN/PAIN11	I in		record enable / safe input (see DIL-SWITCH 81.1)
3	XVSREF/PAIN10	I in		external varispeed frequency
4	-			
5	XVSENB/PAIN9	I in		external varispeed enable
6	REL1			event relay contact 100V/0.3A
7	REL2			event relay contact 100V/0.3A
8	PAOUT6	I out		rehearsal on indication
9	PAOUT7	I out		
10	PAOUT8	I out		
11	+5V			TLS supply voltage
12	PAIN12	I in		rehearsal input
13	PAIN13	I in		(not used)
14	DC			(not used)
15	-			
16	PAIN14	I in		(not used)
17	PAIN15	I in		(not used)
18	PAIN16	I in		(not used)
19	PAIN7	I in		(not used)
20	0.0V			signal GND
21	MVCL	I out		move signal clock
22	SCITX			(not used)
23	SCIRX			(not used)
24	MVDR	I out		move signal direction (LOW = REW)
25	0.0V			signal GND

I out logic output, active low
(open collector, max 30V/0.3A)
I in logic input, active low, optoisolated
(I-low > 10 mA)

Remark: Schematics → see universal parallel IF



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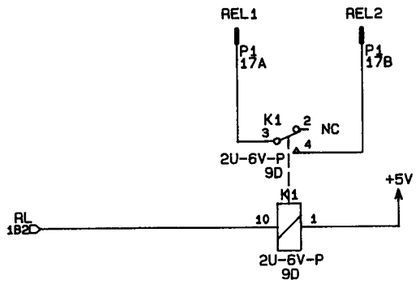
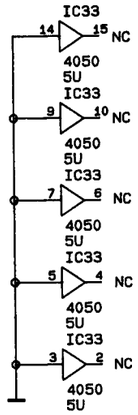
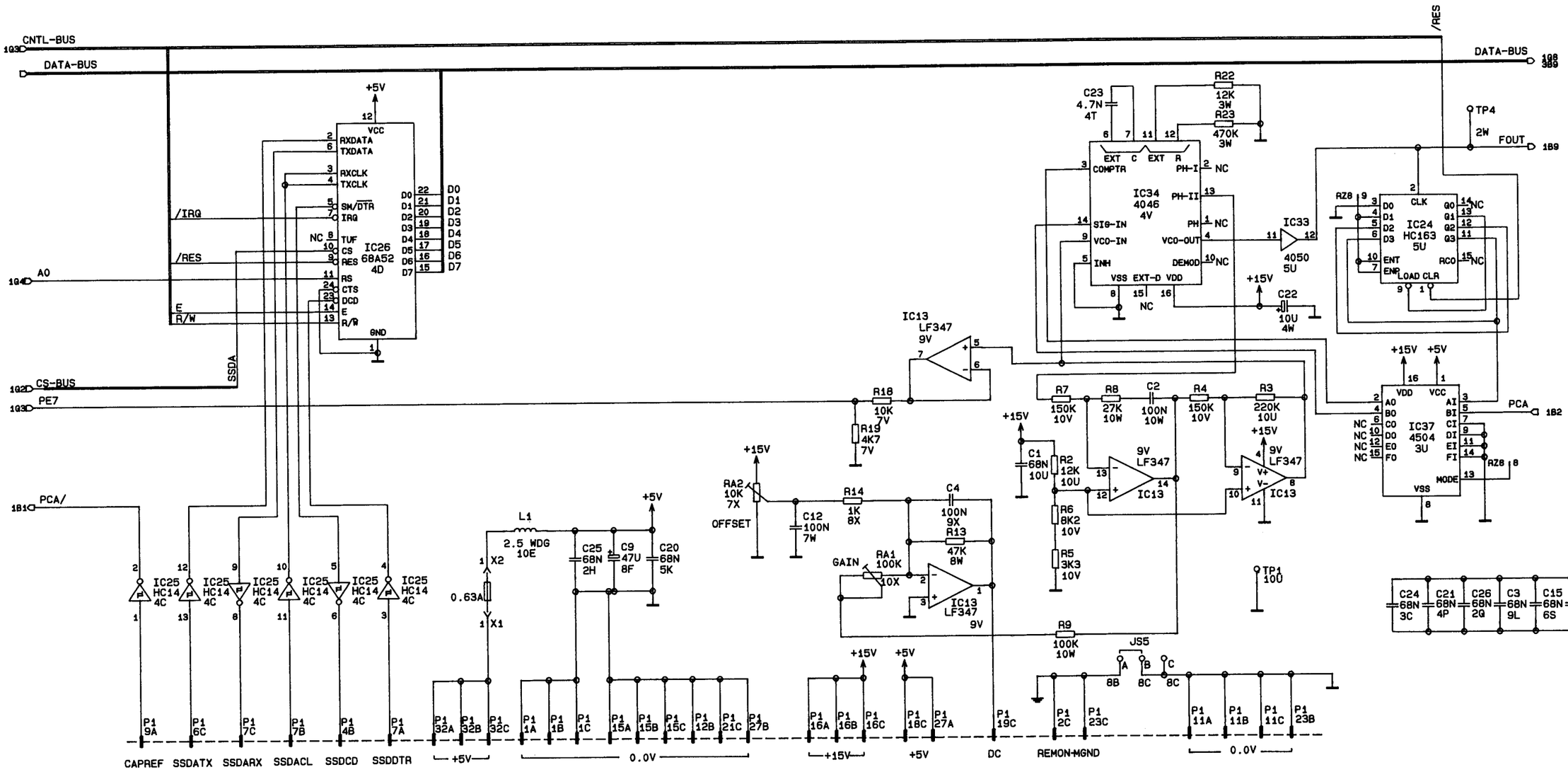
STUDER	TLS PARALLEL INTERFACE ESE			SC	1.812.491-20





VCC = 1

GND = 8



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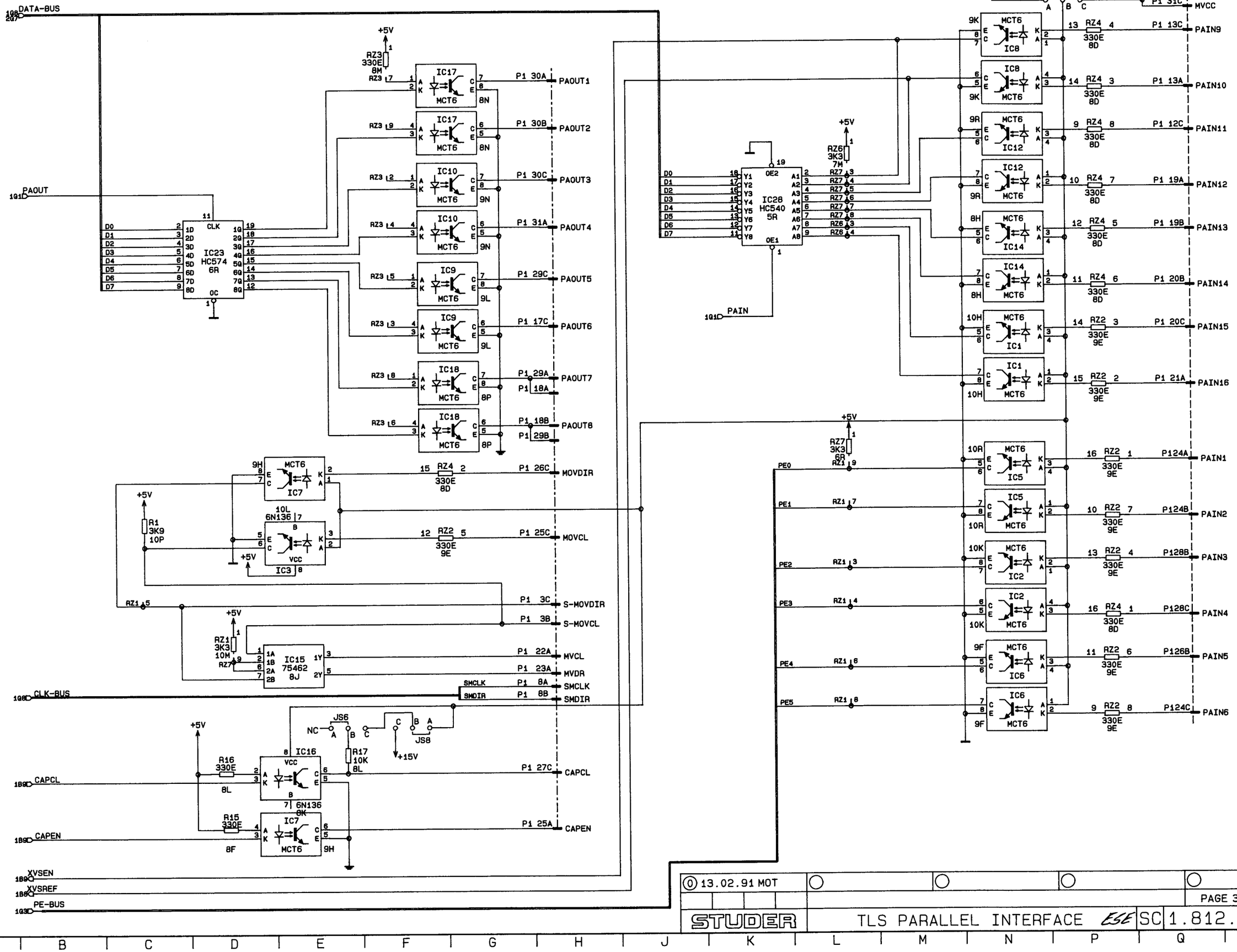

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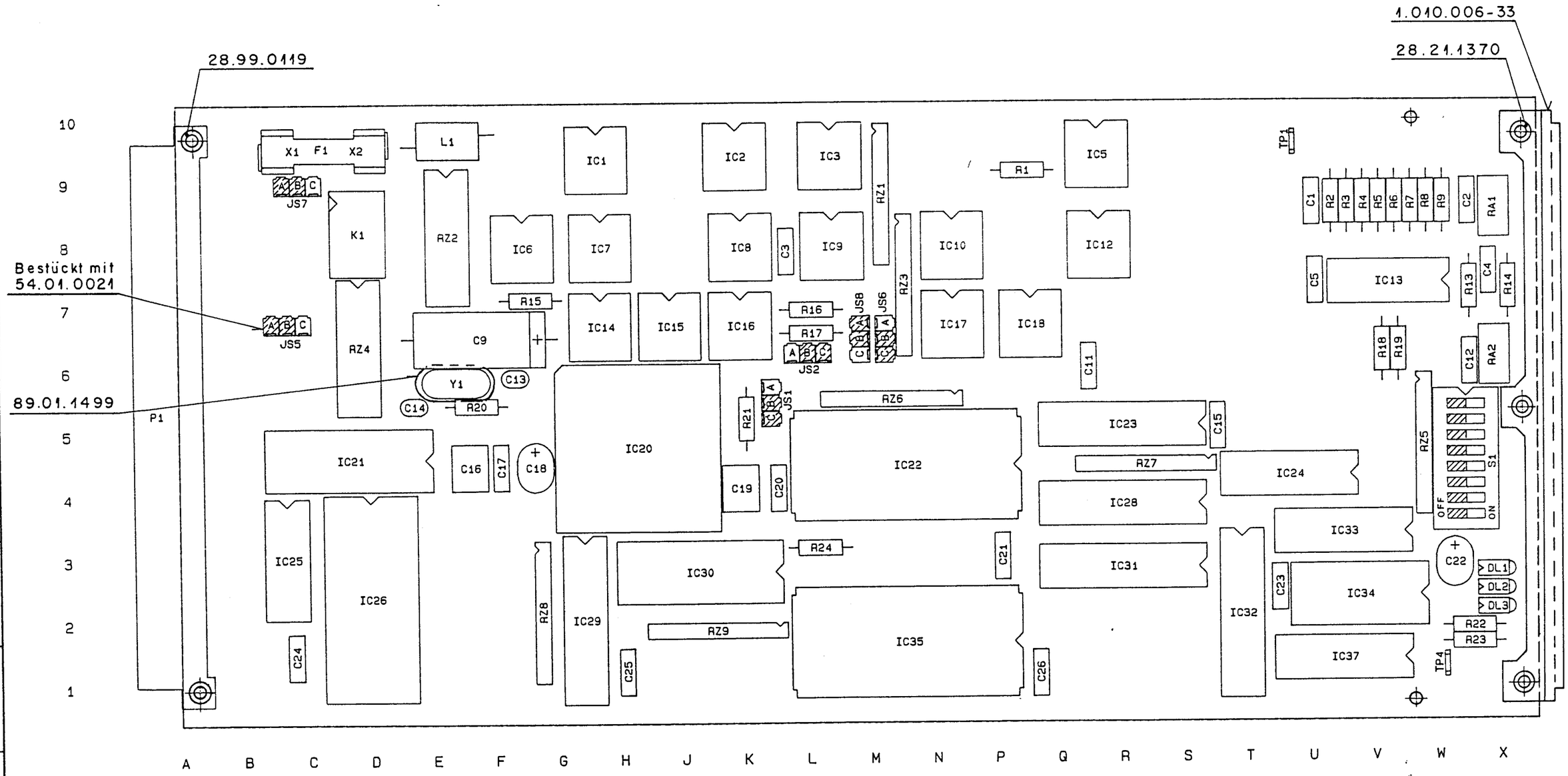

Schilder 43.01.0108 / 1.010.113-51 und 1.812.491-01
aufgeklebt nach Fabrikationsmuster.

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STUDER	TLS PARALLEL INTERFACE ESE				1.812.491-20

TLS4000 Universal Parallel IF 1.812.491.20 (0)

Idx.	Pos.	Part No.	Qty.	Type/Val.	Description
0	C 1	59.06.0683	1 pce	68n	PETP, 63V, 10%, RM5
0	C 2	59.06.0104	1 pce	100n	PETP, 63V, 10%, RM5
0	C 3	59.06.0683	1 pce	68n	PETP, 63V, 10%, RM5
0	C 4	59.06.0104	1 pce	100n	PETP, 63V, 10%, RM5
0	C 5	59.06.0683	1 pce	68n	PETP, 63V, 10%, RM5
0	C 9	59.25.6470	1 pce	47u	EL 63V 20% axial
0	C 11	59.06.0683	1 pce	68n	PETP, 63V, 10%, RM5
0	C 12	59.06.0104	1 pce	100n	PETP, 63V, 10%, RM5
0	C 13	59.34.2220	1 pce	22p	CER 63V, 5%, N150
0	C 14	59.34.2220	1 pce	22p	CER 63V, 5%, N150
0	C 15	59.06.0683	1 pce	68n	PETP, 63V, 10%, RM5
0	C 16	59.06.0105	1 pce	1u0	PETP, 50V, 10%, RM5
0	C 17	59.06.0103	1 pce	10n	PETP, 63V, 10%, RM5
0	C 18	59.26.5100	1 pce	10u	SAL 25V 20%
0	C 19	59.06.0105	1 pce	1u0	PETP, 50V, 10%, RM5
0	C 20	59.06.0683	1 pce	68n	PETP, 63V, 10%, RM5
0	C 21	59.06.0683	1 pce	68n	PETP, 63V, 10%, RM5
0	C 22	59.26.5100	1 pce	10u	SAL 25V 20%
0	C 23	59.06.0472	1 pce	4n7	PETP, 63V, 10%, RM5
0	C 24	59.06.0683	1 pce	68n	PETP, 63V, 10%, RM5
0	C 25	59.06.0683	1 pce	68n	PETP, 63V, 10%, RM5
0	C 26	59.06.0683	1 pce	68n	PETP, 63V, 10%, RM5
0	DL 1	50.04.2107	1 pce	555-2007	DL 555-2007, RT
0	DL 2	50.04.2107	1 pce	555-2007	DL 555-2007, RT
0	DL 3	50.04.2107	1 pce	555-2007	DL 555-2007, RT
0	F 1	51.01.0115	1 pce	630mA	T 5*20 L 250V
0	IC 1	50.99.0111	1 pce	MCT6	DLQ ILD-74, MCT 6, TLP 504 A
0	IC 2	50.99.0111	1 pce	MCT6	DLQ ILD-74, MCT 6, TLP 504 A
0	IC 3	50.04.2163	1 pce	6N136	Optocoupler high speed
0	IC 5	50.99.0111	1 pce	MCT6	DLQ ILD-74, MCT 6, TLP 504 A
0	IC 6	50.99.0111	1 pce	MCT6	DLQ ILD-74, MCT 6, TLP 504 A
0	IC 7	50.99.0111	1 pce	MCT6	DLQ ILD-74, MCT 6, TLP 504 A
0	IC 8	50.99.0111	1 pce	MCT6	DLQ ILD-74, MCT 6, TLP 504 A
0	IC 9	50.99.0111	1 pce	MCT6	DLQ ILD-74, MCT 6, TLP 504 A
0	IC 10	50.99.0111	1 pce	MCT6	DLQ ILD-74, MCT 6, TLP 504 A
0	IC 12	50.99.0111	1 pce	MCT6	DLQ ILD-74, MCT 6, TLP 504 A
0	IC 13	50.09.0104	1 pce	347	IC LF 347 N, ,A
0	IC 14	50.99.0111	1 pce	MCT6	DLQ ILD-74, MCT 6, TLP 504 A
0	IC 15	50.05.0227	1 pce	75462	IC SN 75 472 P, SN 75 462 JG,
0	IC 16	50.04.2163	1 pce	6N136	Optocoupler high speed
0	IC 17	50.99.0111	1 pce	MCT6	DLQ ILD-74, MCT 6, TLP 504 A
0	IC 18	50.99.0111	1 pce	MCT6	DLQ ILD-74, MCT 6, TLP 504 A
0	IC 20	50.63.0004	1 pce	68HC11A1	MPU 8bit 2MHz
0	IC 21	50.18.0100	1 pce	PLD16V8	GAL 8in, 8macrocells
				SW 1.812.998.21	
0	IC 23	50.17.1574	1 pce	74HC574	IC ... 74 HC 574 ., ,A
0	IC 24	50.17.1163	1 pce	74HC163	IC ... 74 HC 163 ., ,A
0	IC 25	50.17.1014	1 pce	74HC 14	IC ... 74 HC 14 ., ,A
0	IC 26	50.16.0114	1 pce	68B52	IC MC68B 52P,MC68 B52
0	IC 28	50.17.1540	1 pce	74HC540	IC ... 74 HC 540 ., ,A
0	IC 29	50.17.1573	1 pce	74HC573	74 HC 573(A)
0	IC 30	50.18.0100	1 pce	PLD16V8	GAL 8in, 8macrocells
				SW 1.812.997.21	
0	IC 31	50.17.1540	1 pce	74HC540	IC ... 74 HC 540 ., ,A
0	IC 32	50.17.1540	1 pce	74HC540	IC ... 74 HC 540 ., ,A
0	IC 33	50.07.0050	1 pce	4050	Hex buffer
0	IC 34	50.07.0046	1 pce	4046	Phase locked loop
0	IC 35	50.14.0133	1 pce	6264	IC HM 6264LP-15
0	IC 37	50.15.0103	1 pce	4504	IC MC14 504 BCP, ,A
0	JS 1	54.01.0020	1 pce	1p	Pin, 1reihig, gerade
0	JS 2	54.01.0020	1 pce	1p	Pin, 1reihig, gerade
0	JS 5	54.01.0020	1 pce	1p	Pin, 1reihig, gerade
0	JS 6	54.01.0020	1 pce	1p	Pin, 1reihig, gerade
0	JS 7	54.01.0020	1 pce	1p	Pin, 1reihig, gerade
0	JS 8	54.01.0020	1 pce	1p	Pin, 1reihig, gerade
0	K 1	56.04.0195	1 pce	2*u	6V 125V 2A Ag/Au
0	L 1	62.01.0115	1 pce	2.5Wdg	Wideband choke
0	P 1	54.01.0358	1 pce	96p	EU-C 3*32p male
0	R 1	57.11.3392	1 pce	3k9	MF, 1%, 0207
0	R 2	57.11.3123	1 pce	12k	MF, 1%, 0207
0	R 3	57.11.3224	1 pce	220k	MF, 1%, 0207
0	R 4	57.11.3154	1 pce	150k	MF, 1%, 0207
0	R 5	57.11.3332	1 pce	3k3	MF, 1%, 0207
0	R 6	57.11.3822	1 pce	8k2	MF, 1%, 0207
0	R 7	57.11.3154	1 pce	150k	MF, 1%, 0207
0	R 8	57.11.3273	1 pce	27k	MF, 1%, 0207
0	R 9	57.11.3104	1 pce	100k	MF, 1%, 0207
0	R 13	57.11.3473	1 pce	47k	MF, 1%, 0207
0	R 14	57.11.3102	1 pce	1k0	MF, 1%, 0207
0	R 15	57.11.3331	1 pce	330R	MF, 1%, 0207
0	R 16	57.11.3331	1 pce	330R	MF, 1%, 0207
0	R 17	57.11.3103	1 pce	10k	MF, 1%, 0207
0	R 18	57.11.3103	1 pce	10k	MF, 1%, 0207
0	R 19	57.11.3472	1 pce	4k7	MF, 1%, 0207
0	R 20	57.11.5475	1 pce	4M7	MF, 5%, 0207
0	R 21	57.11.3102	1 pce	1k0	MF, 1%, 0207
0	R 22	57.11.3123	1 pce	12k	MF, 1%, 0207
0	R 23	57.11.3474	1 pce	470k	MF, 1%, 0207
0	R 24	57.11.3102	1 pce	1k0	MF, 1%, 0207
0	RA 1	58.01.9104	1 pce	100k	Cermet, 10%, 0.5W, vertical
0	RA 2	58.01.9103	1 pce	10k	Cermet, 10%, 0.5W, vertical
0	RZ 1	57.88.4332	1 pce	3k3	8*R Resistor-Netw 2% SIP9
0	RZ 2	57.88.3331	1 pce	330R	8*R Resistor-Netw 2% DIL16
0	RZ 3	57.88.4331	1 pce	330R	8*R Resistor-Netw 2% SIP9
0	RZ 4	57.88.3331	1 pce	330R	8*R Resistor-Netw 2% DIL16
0	RZ 5	57.88.4332	1 pce	3k3	8*R Resistor-Netw 2% SIP9
0	RZ 6	57.88.4332	1 pce	3k3	8*R Resistor-Netw 2% SIP9
0	RZ 7	57.88.4332	1 pce	3k3	8*R Resistor-Netw 2% SIP9
0	RZ 8	57.88.4332	1 pce	3k3	8*R Resistor-Netw 2% SIP9
0	RZ 9	57.88.4332	1 pce	3k3	8*R Resistor-Netw 2% SIP9
0	S 1	55.01.0168	1 pce	8*a	DIL-Switch, PCB
0	TP 1	54.02.0320	1 pce	1p	PCB-Flachst 2.8*0.8, gerade
0	TP 4	54.02.0320	1 pce	1p	PCB-Flachst 2.8*0.8, gerade
0	Y 1	89.01.0560	1 pce	4.9152MHz	XTAL

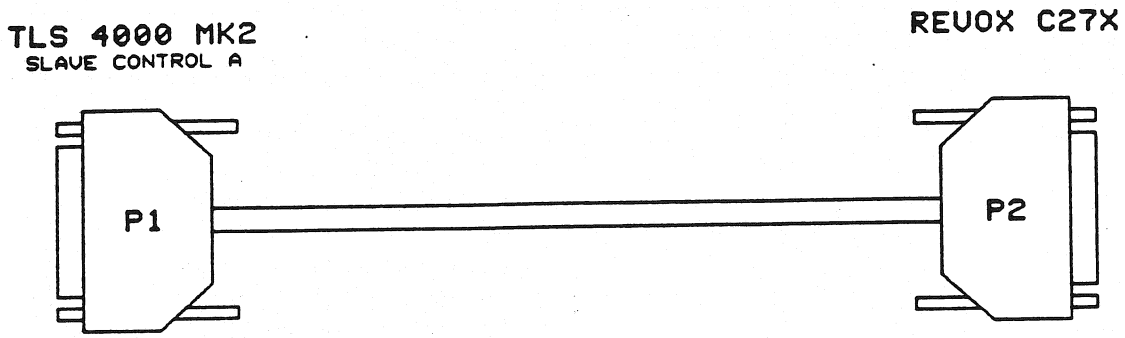
End of List

Comments:

Sockets are used for: IC1...IC22, IC26, IC30, IC35, RZ2, RZ4,

[20] 13.02.91 PG

4.3 IF Cable Description



P1. 1	MGND	P2. 1
2	PAIN1	2
3	PAIN2	3
5	CAPEN	5
7	MOVCL	7
9	PAIN5	9
10	MOVDIR	10
13	CAPCL	13
15	PAIN3	15
16	PAIN4	16
19	PAOUT5	19
20	PAOUT1	20
21	PAOUT2	21
22	PAOUT3	22
23	PAOUT4	23
25	MUCC	25
12	SCREEN	

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